

What is claimed is:

1. A method for determining optimal values of design parameters  
2 of a subsystem to meet design constraints, the subsystem comprising a  
3 plurality of circuits, the method comprising:  
4 (a) creating parameter functions for the corresponding circuits, the  
5 parameter functions representing a relationship among the design  
6 parameters; and  
7 (b) optimizing the design parameters based on the parameter functions  
8 to satisfy the design constraints.

- 1 2. The method of claim 1 wherein the creating the parameter  
2 functions comprises:  
3 (a1) configuring each circuit of the plurality of circuits; and  
4 (a2) generating values of design parameters for each circuit according to  
5 the configured circuit, the values providing the parameter functions.  
1 3. The method of claim 2 wherein the design parameters include  
2 constraint and optimizing sets, the constraint set including constraint  
3 parameters having values selectable to meet the design constraints, the  
4 optimizing set including optimizing parameters having values to be  
5 optimized.

- 1        4.     The method of claim 3 wherein optimizing comprises:
  - 2            (b1) selecting values of the constraint parameters to meet the design
  - 3            constraints;
  - 4            (b2) determining values of the optimizing parameters corresponding to
  - 5            the selected values of the constraint parameters based on the parameter
  - 6            functions; and
  - 7            (b3) iterating (b1) and (b2) until values of the optimizing parameters are
  - 8            within a predetermined optimal range.
- 1        5.     The method of claim 3 wherein the constraint parameters
- 2     include a delay parameter and the optimizing parameters include a power
- 3     parameter.
- 1        6.     The method of claim 5 wherein the design constraints include a
- 2     delay constraint.
- 1        7.     The method of claim 6 wherein (a1) comprises:
  - 2            sizing components in each circuit.

1       8. The method of claim 6 wherein (a1) comprises:

2             selecting a design technology for each circuit, the design technology  
3             being one of static and dynamic technologies.

1       9. The method of claim 7 wherein (a2) comprises:

2             (a21) generating a circuit netlist representing the configured circuit;  
3             (a22) generating a timing file based on the circuit netlist using a circuit  
4             critical path;

5             (a23) determining power of the configured circuit based on the circuit  
6             netlist;

7             (a24) calculating timing values by using a timing simulator; and

8             (a25) calculating power values by using a power estimator.

1       10. The method of claim 9 wherein optimizing comprises:

2             (b1) selecting values of the delay parameter within the delay constraint;  
3             (b2) determining values of the power parameter corresponding to the  
4             selected values of the delay parameter based on the parameter function; and

5             (b3) iterating (b1) and (b2) until values of the power parameter are  
6             within a predetermined optimal range.

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11. A machine readable medium having embodied thereon a  
computer program for processing by a machine, the computer program  
determining optimal values of design parameters of a subsystem to meet  
design constraints, the subsystem comprising a plurality of circuits, the  
computer program comprising:

(a) a first code segment for creating parameter functions for the  
corresponding circuits, the parameter functions representing a  
relationship among the design parameters; and

(b) a second code segment for optimizing the design parameters  
based on the parameter functions to satisfy the design constraints.

12. The machine readable medium of claim 11 wherein the first  
code segment comprises:

(a1) a code segment for configuring each circuit of the plurality of  
circuits; and

(a2) a code segment for generating values of design parameters for each  
circuit according to the configured circuit, the values providing the parameter  
functions.

13. The machine readable medium of claim 12 wherein the design  
parameters include constraint and optimizing sets, the constraint set

3 including constraint parameters having values selectable to meet the design  
4 constraints, the optimizing set including optimizing parameters having  
5 values to be optimized.

1           14. The machine readable medium of claim 13 wherein the second  
2 code segment comprises:

3           (b1) a code segment for selecting values of the constraint parameters to  
4 meet the design constraints;

5           (b2) a code segment for determining values of the optimizing  
6 parameters corresponding to the selected values of the constraint parameters  
7 based on the parameter functions; and

8           (b3) a code segment for iterating (b1) and (b2) until values of the  
9 optimizing parameters are within a predetermined optimal range.

1           15. The machine readable medium of claim 13 wherein the  
2 constraint parameters include a delay parameter and the optimizing  
3 parameters include a power parameter.

1           16. The machine readable medium of claim 15 wherein the design  
2 constraints include a delay constraint.

1        17. The machine readable medium of claim 16 wherein (a1)  
2 comprises:

3            a code segment for sizing components in each circuit.

1        18. The machine readable medium of claim 16 wherein (a1)  
2 comprises:

3            a code segment for selecting a design technology for each circuit, the  
4 design technology being one of static and dynamic technologies.

1        19. The machine readable medium of claim 18 wherein (a2)  
2 comprises:

3            (a21) a code segment for generating a circuit netlist representing the  
4 configured circuit;

5            (a22) a code segment for generating a timing file based on the circuit  
6 netlist using a circuit critical path;

7            (a23) a code segment for determining power vectors of the configured  
8 circuit based on the circuit netlist;

9            (a24) a code segment for calculating timing values; and

10          (a25) a code segment for calculating power values.

1        20. The machine readable medium of claim 19 wherein the second  
2 code segment comprises:

3            (b1) a code segment for selecting values of the delay parameter within  
4 the delay constraints;

5            (b2) a code segment for determining values of the power parameter  
6 corresponding to the selected values of the delay parameter based on the  
7 parameter function; and

8            (b3) a code segment for iterating (b1) and (b2) until values of the power  
9 parameter are within a predetermined optimal range.

*b6 b7 Q5* 21. A system comprising:  
a computer for determining optimal values of design parameters of a  
subsystem to meet design constraints, the subsystem comprising a plurality of  
circuits; and  
a design environment incorporated in the computer for providing  
tools to facilitate determining the optimal values of the design parameters.

1        22. The system of claim 21 wherein the computer system comprises:  
2            a memory for storing program instructions;

3           a processor coupled to the memory for executing the program  
4 instructions, the program instructions when executed by the processor  
5 interacting with the tools provided by the design environment to at least  
  
6           (a) create parameter functions for the corresponding circuits, the  
7 parameter functions representing a relationship among the design  
8 parameters, and  
  
9           (b) optimize the design parameters based on the parameter  
10 functions to satisfy the design constraints.

1           23.     The system of claim 22 wherein the parameter functions are  
2 created by:  
  
3           (a1) configuring each circuit of the plurality of circuits; and  
  
4           (a2) generating values of design parameters for each circuit according to  
5 the configured circuit, the values providing the parameter functions.  
  
1           24.     The system of claim 22 wherein the design parameters include  
2 constraint and optimizing sets, the constraint set including constraint  
3 parameters having values selectable to meet the design constraints, the  
4 optimizing set including optimizing parameters having values to be  
5 optimized.

1        25. The system of claim 24 wherein the design parameters are  
2 optimized by:

3            (b1) selecting values of the constraint parameters to meet the design  
4 constraints;

5            (b2) determining values of the optimizing parameters corresponding to  
6 the selected values of the constraint parameters based on the parameter  
7 functions; and

8            (b3) iterating (b1) and (b2) until values of the optimizing parameters are  
9 within a predetermined optimal range.

1        26. The system of claim 24 wherein the constraint parameters  
2 include a delay parameter and the optimizing parameters include a power  
3 parameter.

1        27. The system of claim 26 wherein the design constraints include a  
2 delay constraint.

*add C8*